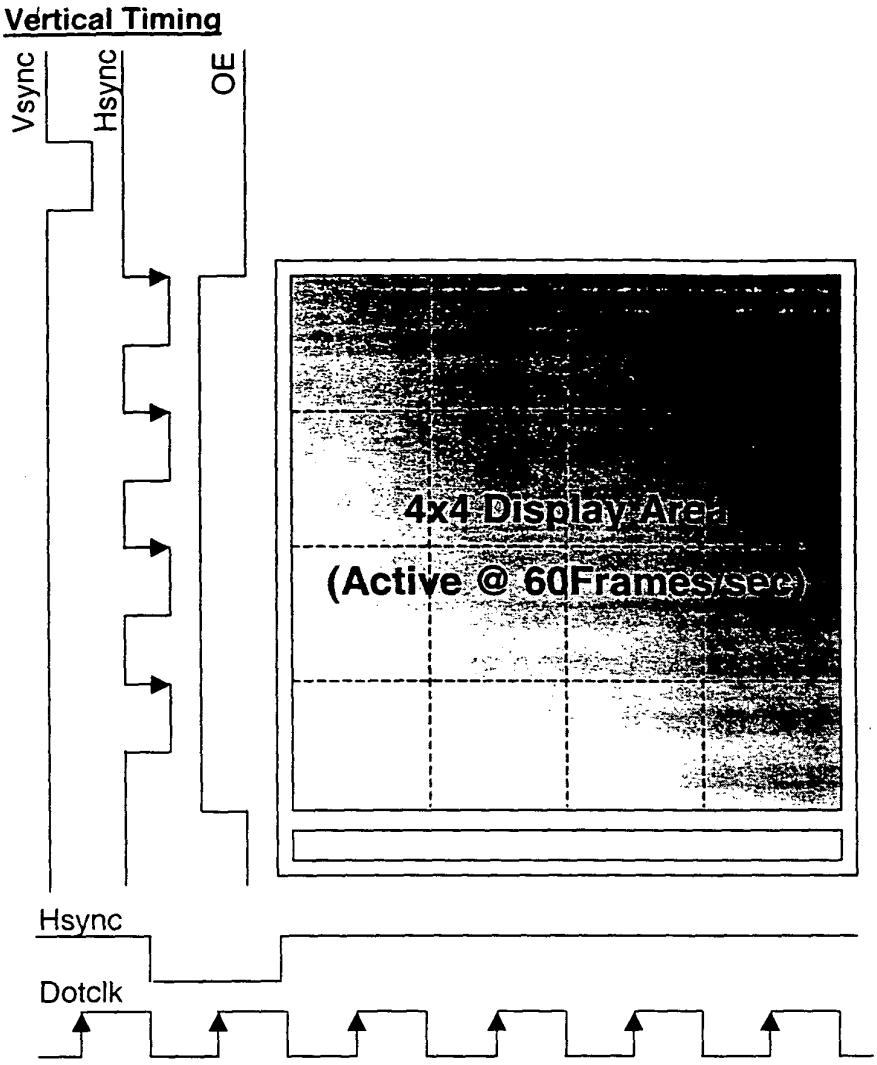
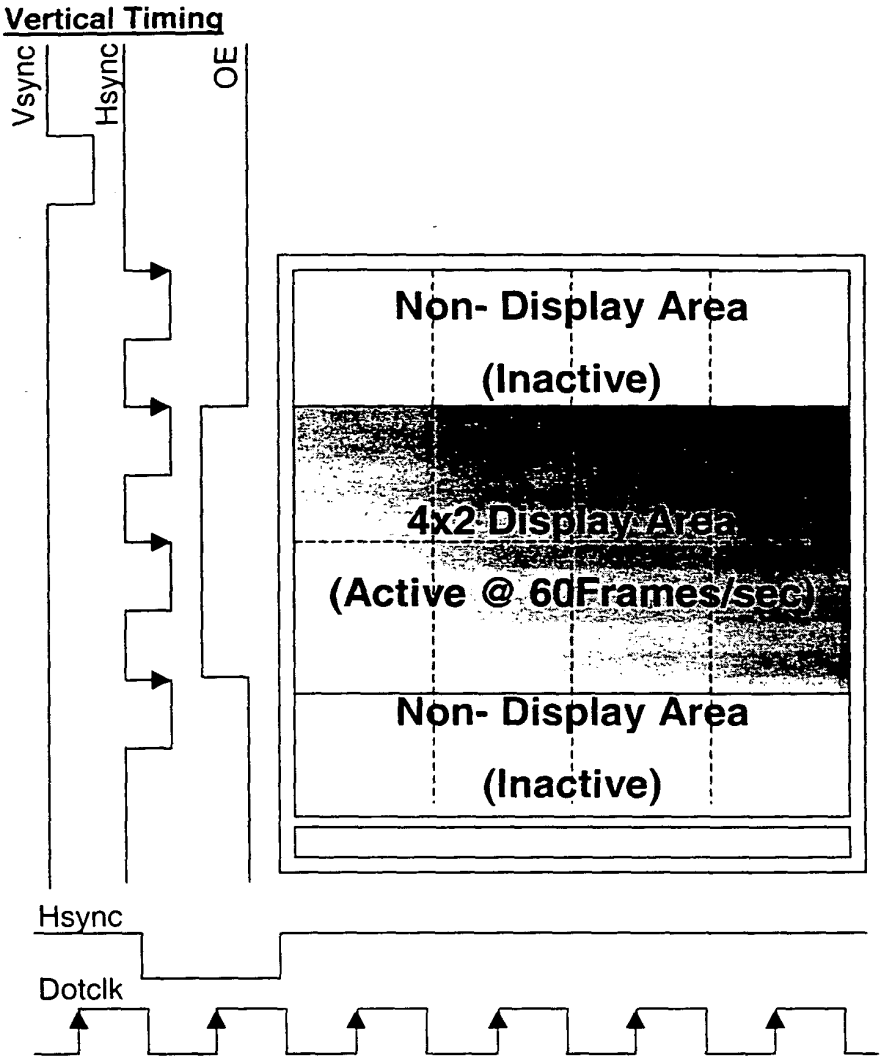


(PRIOR ART) **Fig 1**

C322497RA-FCC



(PRIOR ART) **Fig 2**

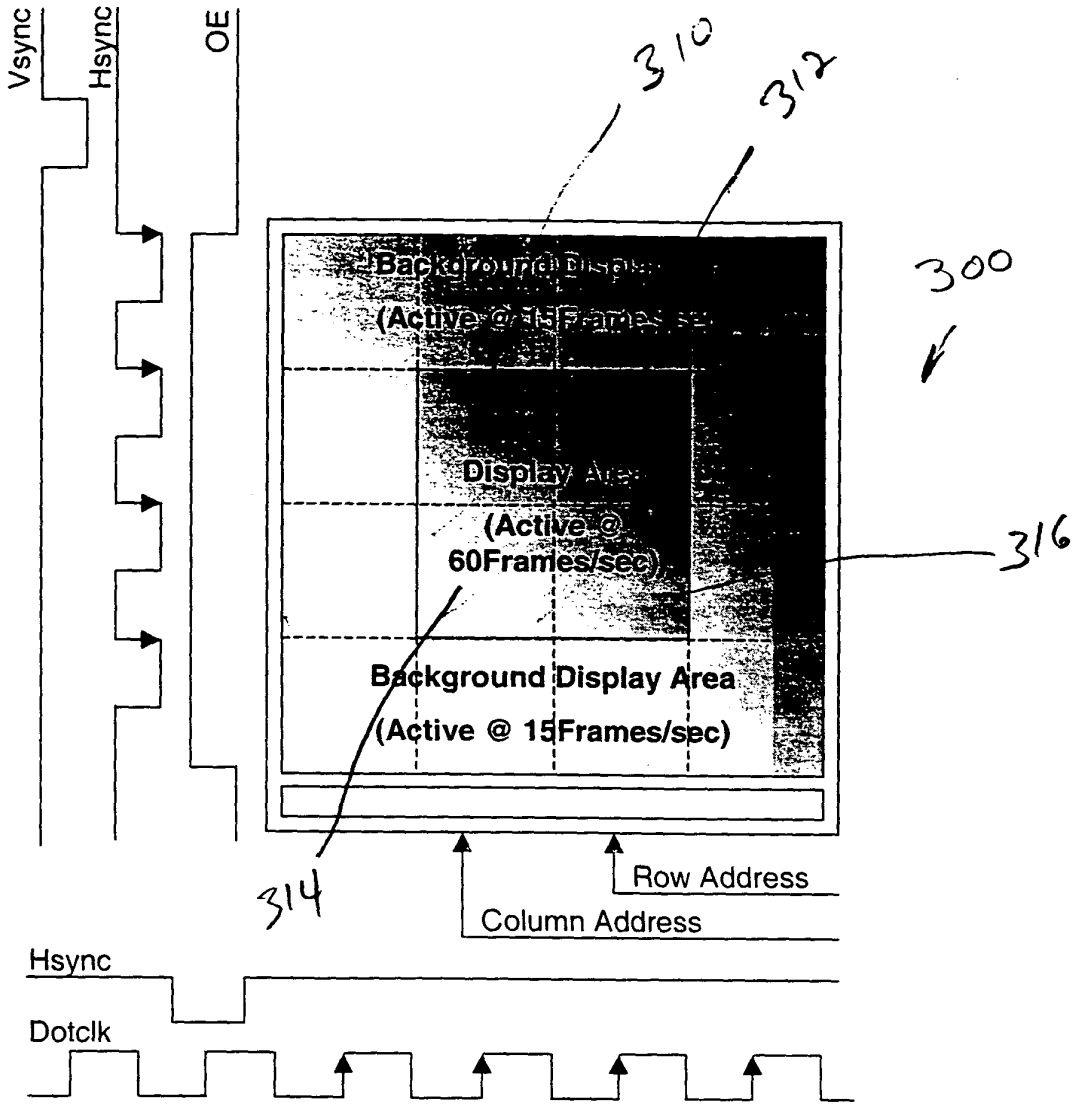

Vsync
Hsync
OE
310
312
300
Background Display
(Active @ 15Frames/sec)
Display Area
(Active @
60Frames/sec)
316
Background Display Area
(Active @ 15Frames/sec)
314
Row Address
Column Address
Hsync
Dotclk

Fig 3

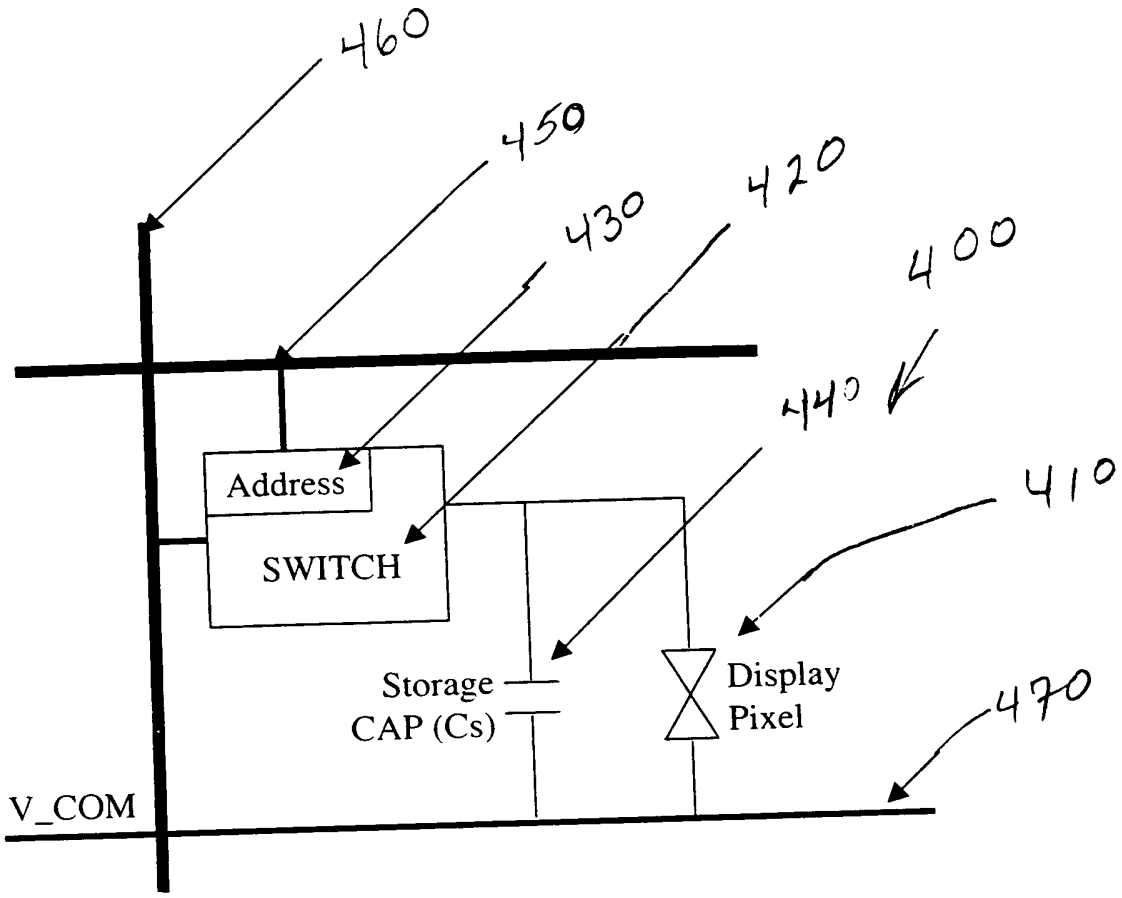

460
450
430
420
400
440
410
Address
SWITCH
Storage
CAP (Cs)
Display
Pixel
470
V_COM

Fig 4

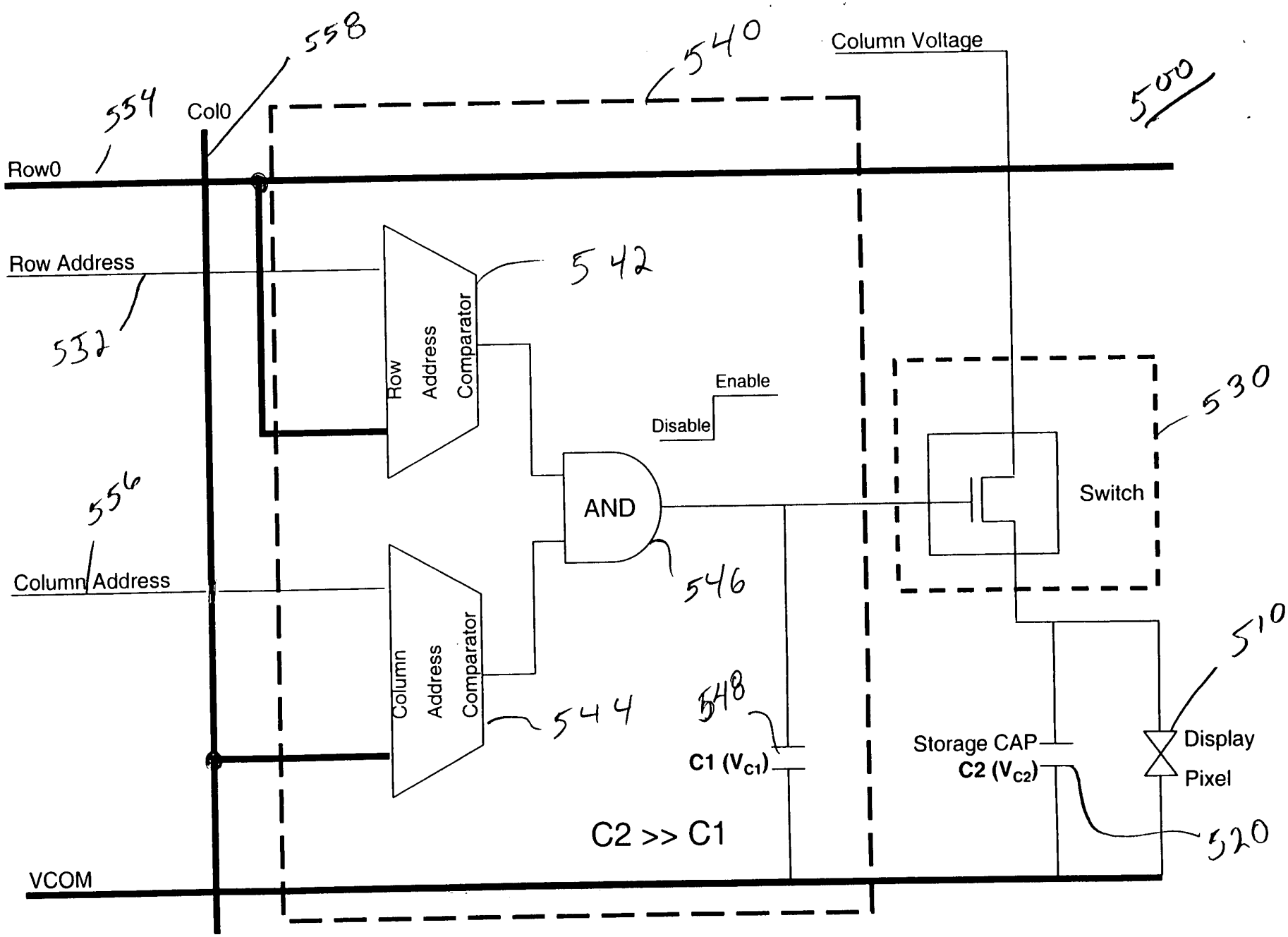

558
540
Column Voltage
554
Col0
500
Row0
Row Address
542
532
Row Address Comparator
Enable
Disable
530
AND
Switch
556
Column Address
546
Column Address Comparator
544
548
510
C1 (V_{C1})
Storage CAP
C2 (V_{C2})
Display Pixel
C2 >> C1
520
VCOM

Fig 5

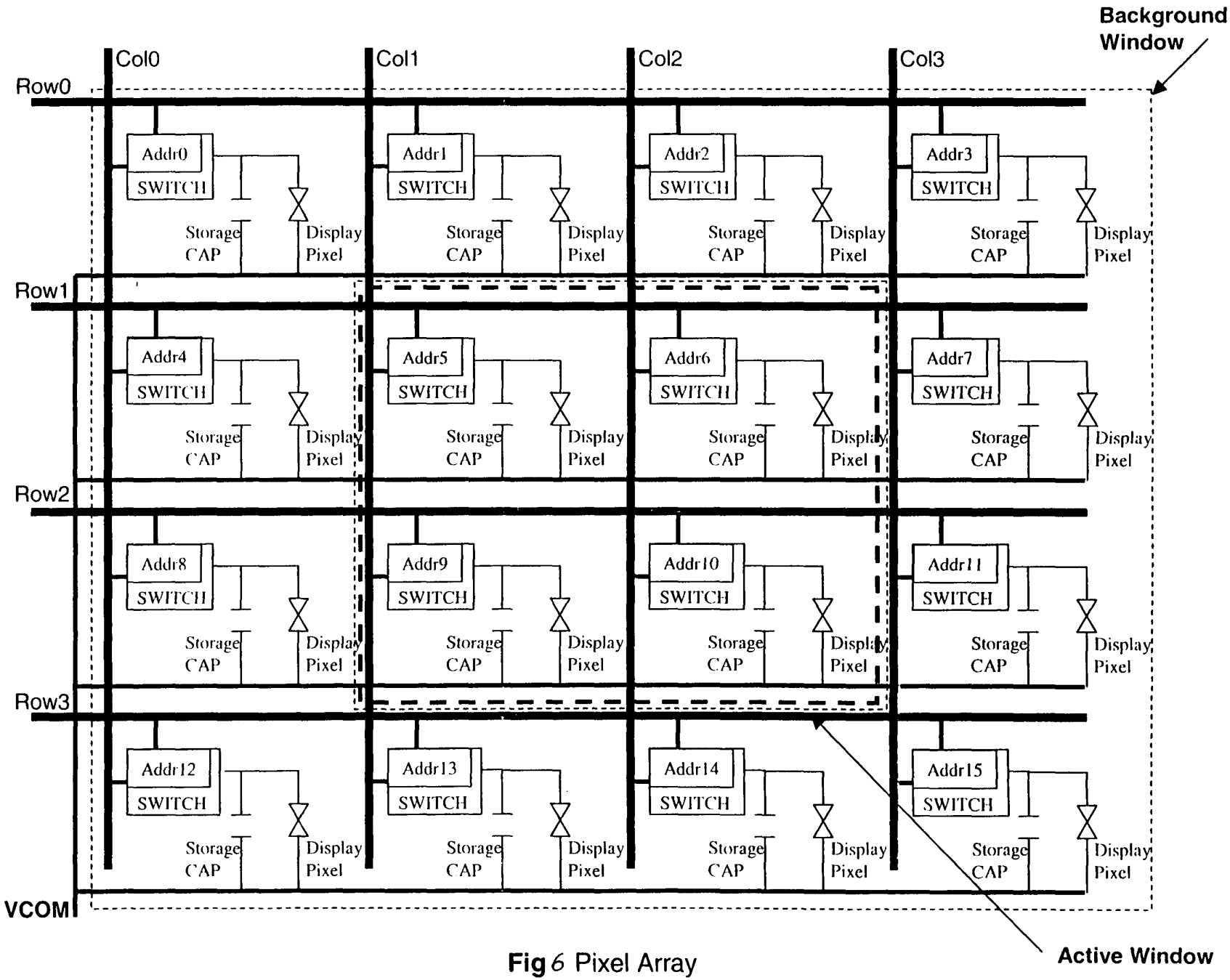


Fig *6* Pixel Array

Fig 7

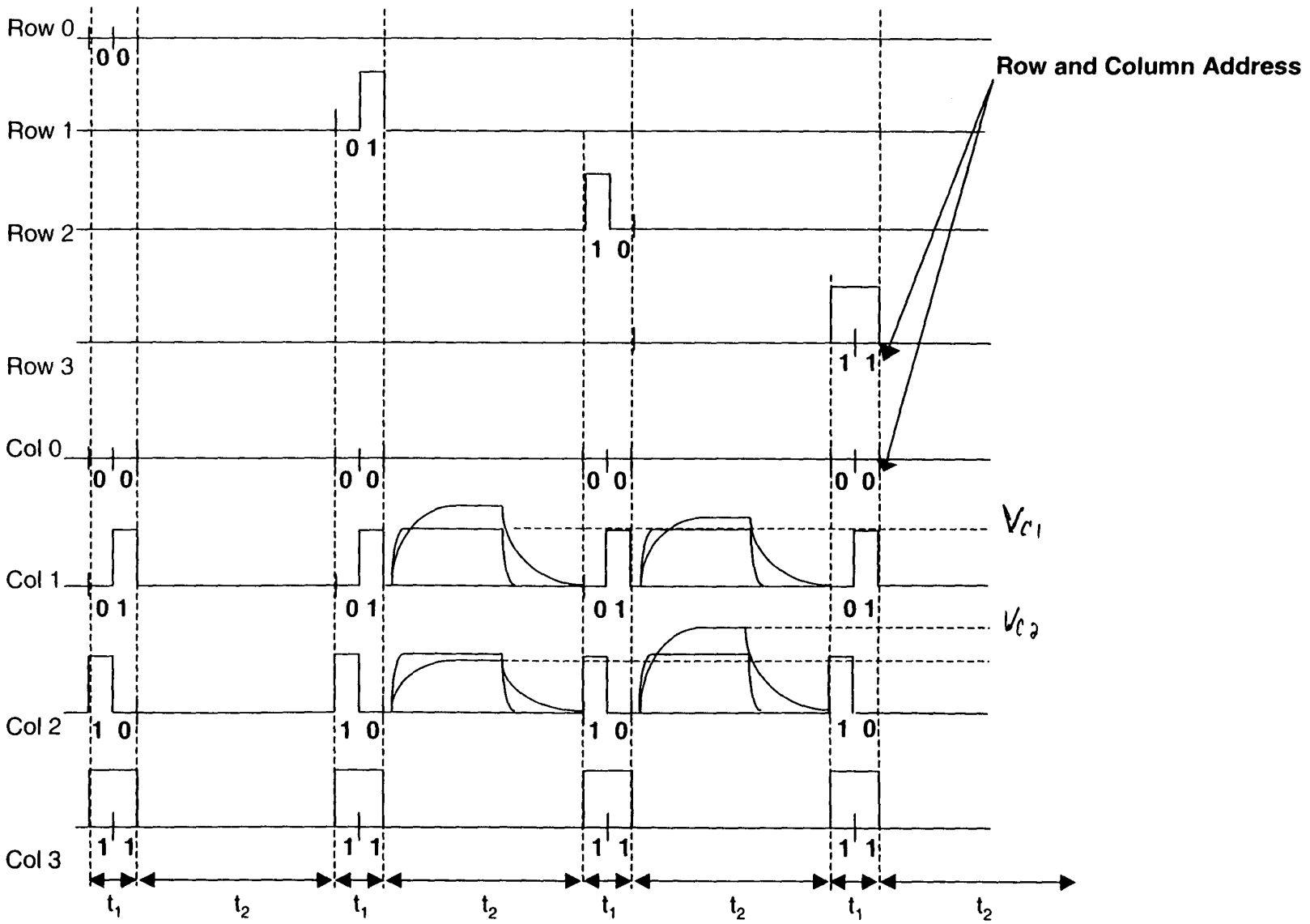
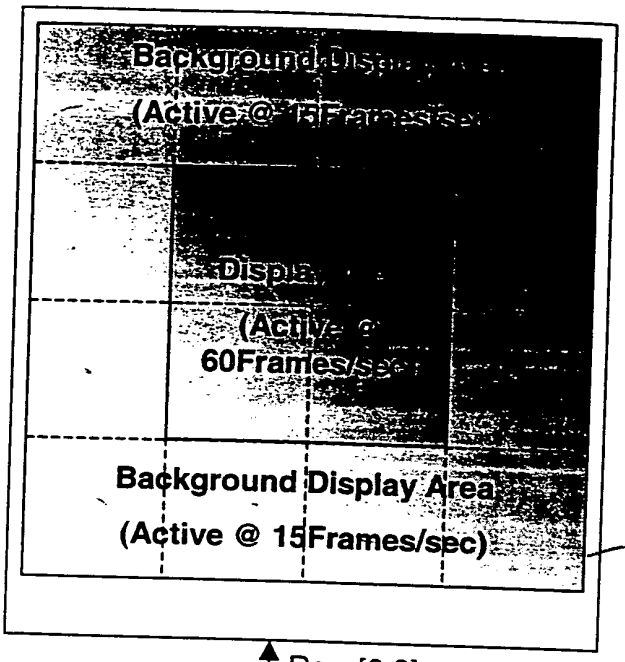

Row 0
Row 1
Row 2
Row 3
Col 0
Col 1
Col 2
Col 3
Row and Column Address
V_{c1}
V_{c2}
0 0
0 1
1 0
1 1
t_1
t_2

FIG 8



800

840

Row [0:3] waveforms

Column [0:3] waveforms

Driver IC

820

Vsync, Hsync, Dotclk, OE

Row Address, Column Address

Timing Signal Generator

810

6800/8080 (Parallel or Serial I/F)

Baseband Microprocessor

830